

TABLE 1

| 20 Pin PDIP, SOIC | 20 Pin SSOP | Name | Input Type | Pull-up/ Current Source | Output Type | Description |
|-------------------------|----------------|--------|---------------|-------------------------------|----------------|---|
| 1 | 1 | RA0 | ST | N/A | — | Port Input |
| | | AN0 | AN | — | — | ADC Input |
| | | OPA+ | AN | — | — | Op Amp Non-inverting Input |
| 2 | 2 | RA1 | ST | N/A | — | Port Input |
| | | AN1 | AN | — | — | ADC Input |
| | | OPA- | AN | — | — | Op amp Inverting Input |
| 7 | 7 | RA2 | ST | CMOS | — | Bi-directional I/O |
| | | AN2 | AN | — | — | ADC Input |
| | | Vref2 | AN | — | — | Voltage Reference Input for C2 Comparator |
| 8 | 8 | RA3 | ST | CMOS | — | Bi-directional I/O |
| | | AN3 | AN | — | — | ADC Input |
| | | Vref1 | AN | — | — | Voltage Reference Input for C1 Comparator, ADC, and DAC Modules |
| 3 | 3 | RA4 | ST | OD | — | Bi-directional I/O |
| | | TOCKI | ST | — | — | To Clock Input |
| 4 | 4 | RA5 | ST | — | — | Port Input |
| | | MCLR | ST | No | — | Master Clear Input |
| | | Vpp | Power | — | — | Programming Voltage |
| 17 | 17 | RA6 | ST | CMOS | — | Bi-directional I/O |
| | | OSC2 | — | Xtal | — | Crystal/Resonator |
| | | CLKOUT | — | CMOS | — | Internal Clock (Fosc/4) Output |
| 18 | 18 | RA7 | ST | CMOS | — | Bi-directional I/O |
| | | OSC1 | Xtal | — | — | Crystal/Resonator |
| | | CLKIN | ST | — | — | External Clock Input Connection. |
| | | T1CKI | ST | — | — | Timer1 External Clock Input |

TABLE 1 (cont'd)

| 20 Pin PDP, SOIC | | 20 Pin SSOP | Name | Input Type | Pull-up/ Current Source | Output Type | Description |
|------------------|----|-------------|-------|------------|-------------------------|--|-------------|
| 9 | 9 | RB0 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| | | INT | ST | — | — | Interrupt | |
| | | AN4 | AN | — | — | ADC, C1, or C2 Comparator Input | |
| | | VREF | | AN | — | VREF Reference Output | |
| 10 | 10 | RB1 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| | | AN5 | AN | — | — | ADC, C1, or C2 Comparator Input | |
| | | VDAC | | AN | — | DAC Output | |
| 19 | 19 | RB2 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| | | AN6 | AN | — | — | ADC, C1, or C2 Comparator Input | |
| 20 | 20 | RB3 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| | | AN7 | AN | — | — | ADC, C1, or C2 Comparator Input | |
| | | OPA | | AN | — | Op Amp Output | |
| 11 | 11 | RB4 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| 12 | 12 | RB5 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| 13 | 13 | RB6 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| | | PSMC1A | | CMOS | — | PSMC1A Output | |
| | | C1 | | CMOS | — | C1 Comparator Output | |
| 14 | 14 | RB7 | TTL | RBPUs | CMOS | Bi-directional I/O with Selectable Pull-up and Interrupt on Change | |
| | | PSMC1B | | CMOS | — | PSMC1B Output | |
| | | C2 | | CMOS | — | C2 comparator Output | |
| | | T1G | ST | — | — | Timer1 Gate Input | |
| 16 | 16 | Vdd | Power | — | — | Digital Power | |
| 5 | 5 | Vss | Power | — | — | Digital Ground | |
| 15 | 15 | AVdd | Power | — | — | Analog Power | |
| 6 | 6 | AVss | Power | — | — | Analog Ground | |

Legend: ST=Schmitt Trigger Input Voltage Levels, CMOS=Complimentary Metal Oxide Semiconductor Output Voltage Levels, TTL=Transistor Transistor Logic Input Voltage Levels, AN=Analog I/O Voltage Levels, OD=Open Drain Output, Xtal=Crystal, RBBPU=Port B Pull-Up

TABLE 2A

| Alternate Function | PORTA (when not in digital I/O) | | | | | | | |
|------------------------|---------------------------------|-------------|------|-------|-------------|-------------|-------------------------|-------------------------|
| | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| Low Leakage Input only | — | — | — | — | — | — | < 60pA (tested to 50nA) | < 60pA (tested to 50nA) |
| ADC | — | — | — | — | AN3 | AN2 | AN1 | AN0 |
| Op Amp | — | — | — | — | — | — | OPA- Input | OPA+ Input |
| VREF Inputs | — | — | — | — | VREF2 Input | VREF1 Input | — | — |
| Timer0 | — | — | — | T0CKI | — | — | — | — |
| Timer1 | T1CKI | — | — | — | — | — | — | — |
| Oscillator | OSC1/CLKIN | OSC2/CLKOUT | — | — | — | — | — | — |
| Reset | — | — | MCLR | — | — | — | — | — |
| Programming | — | — | Vpp | — | — | — | — | — |

Note 1: Dashed cell implies that the Alternate Function does not apply.

TABLE 2B

| Alternate Function | PORTB (when not in digital I/O) | | | | | | | |
|--------------------|---------------------------------|---------------|-----|-----|------------|-----|-----|-------------|
| | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
| INT | — | — | — | — | — | — | — | INT |
| ADC | — | — | — | — | AN7 | AN6 | AN5 | AN4 |
| Op amp | — | — | — | — | OPA Output | — | — | — |
| C2 comparator | C2 Output | — | — | — | AN7 | AN6 | AN5 | AN4 |
| C1 comparator | — | C1 Output | — | — | AN7 | AN6 | AN5 | AN4 |
| VREF Reference | — | — | — | — | — | — | — | VREF Output |
| DAC | — | — | — | — | — | — | — | VDAC Output |
| PSMC | PSMC1B Output | PSMC1A Output | — | — | — | — | — | — |
| Timer1 | T1G Input | — | — | — | — | — | — | — |
| Programming | Data | Clock | — | — | — | — | — | — |

Note 1: Dashed cell implies that the Alternate Function does not apply.

TABLE 3

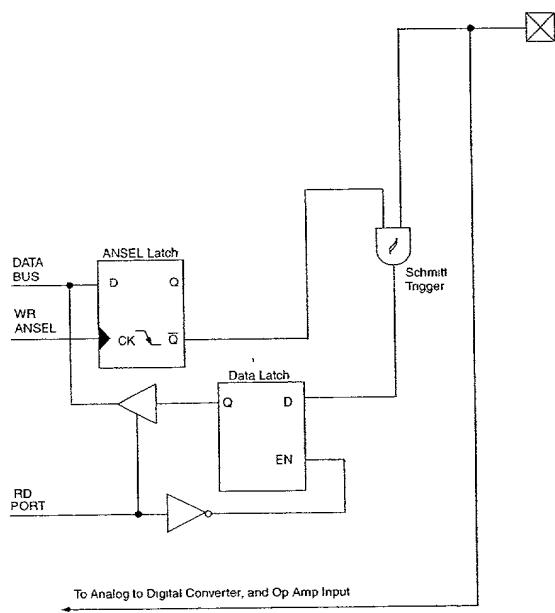
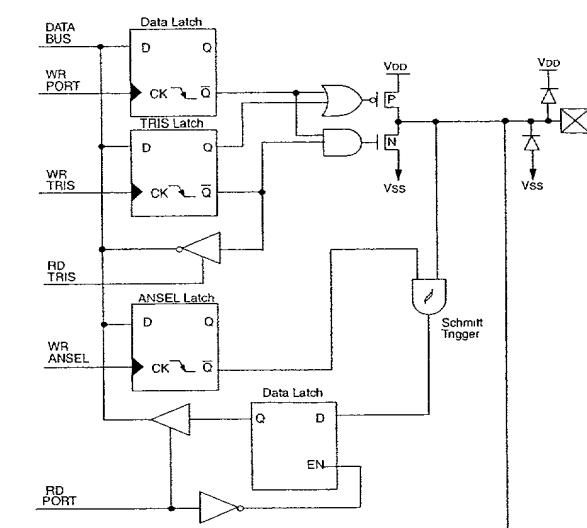
| PIN NAME | EXEMPLARY BLOCK CIRCUITY |
|---------------------------------|---|
| RA0/AN0/OPA+, RA1/AN1/OPA- |  <p>To Analog to Digital Converter, and Op Amp Input</p> |
| RA2/AN2/VREF2 AND RA3/AN3/VREF1 |  <p>To Analog to Digital Converter and VREF1 or VREF2 input</p> |

TABLE 3 (cont'd)

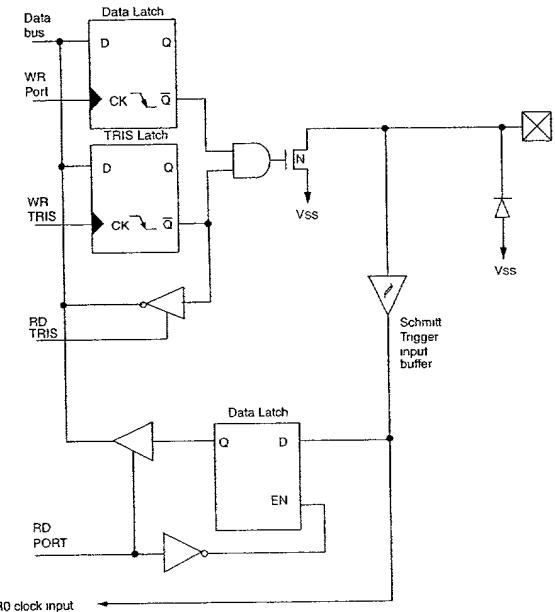
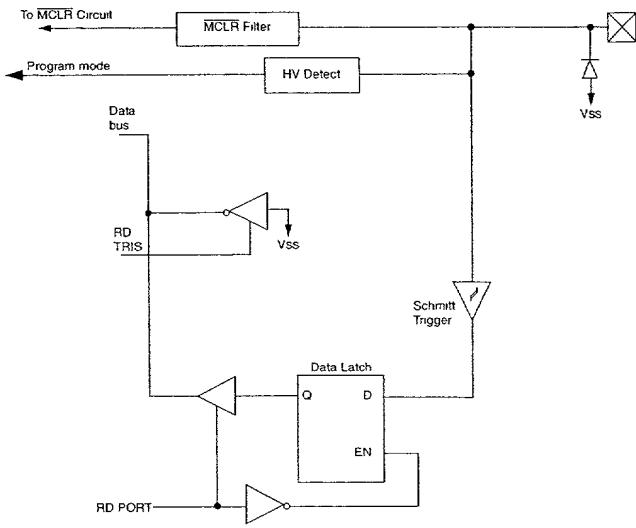
| PIN NAME | EXEMPLARY BLOCK CIRCUITY |
|--------------|---|
| RA4/T0CKI |  <p>RA4/T0CKI</p> <p>This circuit diagram illustrates the internal logic for the RA4/T0CKI pin. It features two data latches (one with CK and Q, the other with CK and \bar{Q}) and a TRIS latch (also with CK and Q/\bar{Q} outputs). The RD TRIS signal is inverted and used as an enable for a third data latch (Q to D, EN). The RD PORT signal is inverted and used as an enable for a fourth data latch (Q to D, EN). A Schmitt Trigger input buffer is connected to the RD PORT signal. The TMR0 clock input is also connected to the RD PORT signal. The WR Port and WR TRIS signals are connected to the CK inputs of the top two latches. The RD TRIS signal is connected to the CK input of the third latch. The RD PORT signal is connected to the CK input of the fourth latch. The outputs of the latches are connected to a logic block that generates the RD PORT signal and the TMR0 clock input. The outputs of the latches are also connected to a Schmitt Trigger input buffer, which is connected to the RD PORT signal. The outputs of the latches are also connected to a logic block that generates the RD PORT signal and the TMR0 clock input. The outputs of the latches are also connected to a Schmitt Trigger input buffer, which is connected to the RD PORT signal.</p> |
| RA5/MCLR/VPP |  <p>RA5/MCLR/VPP</p> <p>This circuit diagram illustrates the internal logic for the RA5/MCLR/VPP pin. It includes an MCLR Filter, an HV Detect block, and a Schmitt Trigger input buffer. The RD TRIS signal is inverted and connected to the RD PORT signal. The RD PORT signal is connected to the CK input of a data latch (Q to D, EN). The RD TRIS signal is also connected to the CK input of a second data latch (Q to D, EN). The outputs of these two latches are connected to a logic block that generates the RD PORT signal and the MCLR signal. The MCLR signal is connected to the MCLR Filter, which is connected to the RD PORT signal. The RD PORT signal is also connected to the HV Detect block, which is connected to the RD PORT signal. The RD PORT signal is also connected to the Schmitt Trigger input buffer, which is connected to the RD PORT signal.</p> |

TABLE 3 (cont'd)

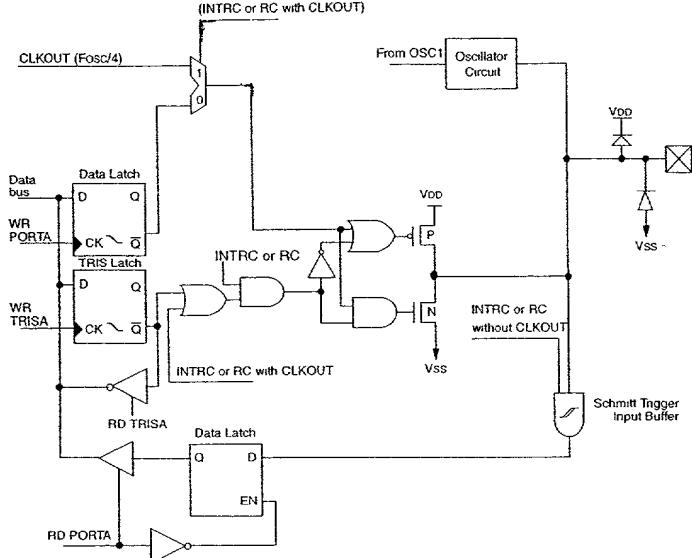
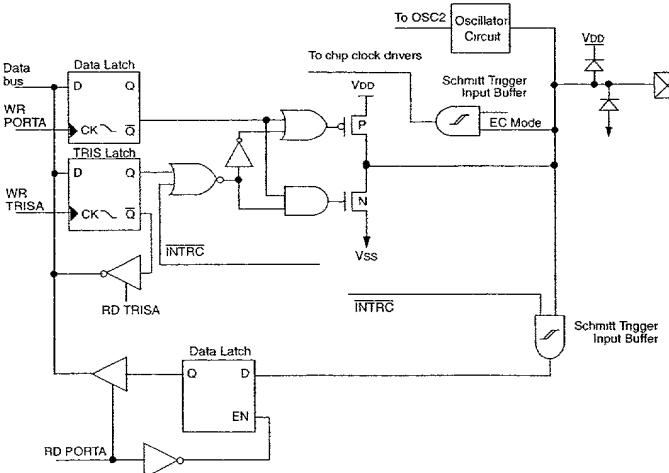
| PIN NAME | EXEMPLARY BLOCK CIRCUITRY |
|-----------------|--|
| RA6/OSC2/CLKOUT |  <p>Diagram illustrating the exemplary block circuitry for RA6/OSC2/CLKOUT. The circuit includes:</p> <ul style="list-style-type: none"> Data Latches: Two latches (Data Latch and TRIS Latch) with D inputs connected to the Data bus and Q outputs. CK inputs are controlled by WR PORTA and WR TRISA respectively. RD TRISA controls the RD PORTA output. OSCILLATOR: An oscillator circuit (From OSC1) provides a clock signal to the Data Latch and TRIS Latch. It also drives an inverter and a Schmitt Trigger Input Buffer. INTERRUPT LOGIC: The Q outputs of the latches are connected to an AND gate. The output of this gate is connected to an inverter and a second AND gate. The output of the second AND gate is connected to a Schmitt Trigger Input Buffer. The output of the Schmitt Trigger Input Buffer is labeled "INTRC or RC without CLKOUT". POWER SUPPLY: VDD and VSS connections are shown, with diodes and switches for power management. |
| RA7/OSC1/CLKIN |  <p>Diagram illustrating the exemplary block circuitry for RA7/OSC1/CLKIN. The circuit includes:</p> <ul style="list-style-type: none"> Data Latches: Two latches (Data Latch and TRIS Latch) with D inputs connected to the Data bus and Q outputs. CK inputs are controlled by WR PORTA and WR TRISA respectively. RD TRISA controls the RD PORTA output. OSCILLATOR: An oscillator circuit (To OSC2) provides a clock signal to the Data Latch and TRIS Latch. It also drives an inverter and a Schmitt Trigger Input Buffer. INTERRUPT LOGIC: The Q outputs of the latches are connected to an AND gate. The output of this gate is connected to an inverter and a second AND gate. The output of the second AND gate is connected to a Schmitt Trigger Input Buffer. The output of the Schmitt Trigger Input Buffer is labeled "INTRC". POWER SUPPLY: VDD and VSS connections are shown, with diodes and switches for power management. |

TABLE 3 (cont'd)

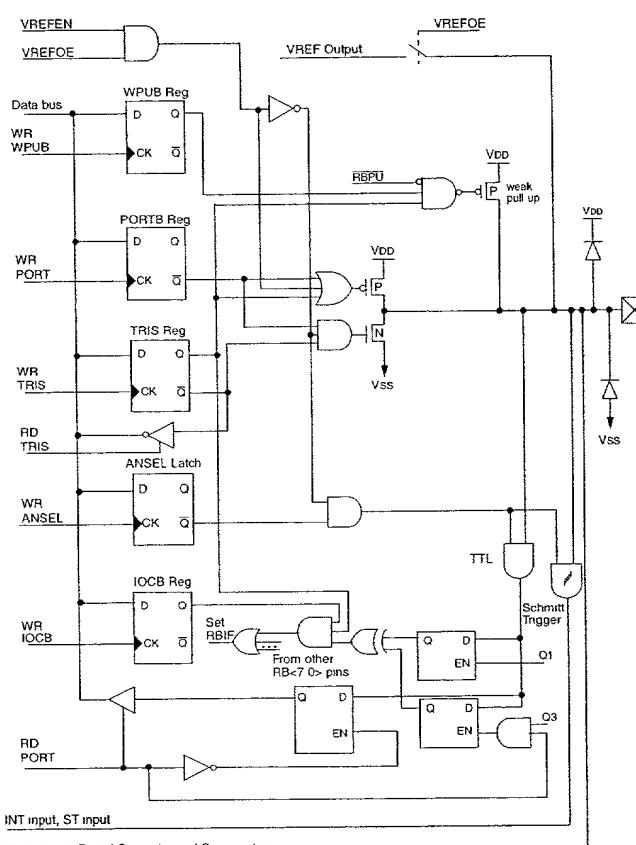
| PIN NAME | EXEMPLARY BLOCK CIRCUITY |
|------------------|--|
| RB0/INT/AN4/VREF |  <p>INT input, ST input</p> <p>To Analog to Digital Converter and Comparators</p> |

TABLE 3 (cont'd)

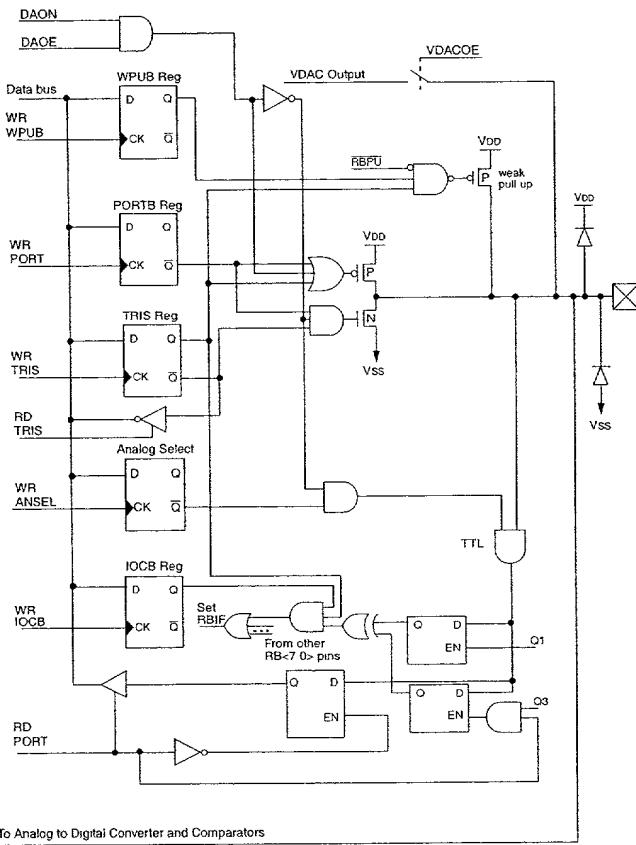
| PIN NAME | EXEMPLARY BLOCK CIRCUITY |
|--------------|--|
| RB1/AN5/VDAC |  <p>RB1/AN5/VDAC</p> <p>DAON, DAOE, WR_WPUB, WR_PORT, RD_TRIS, WR_ANSEL, WR_ICOB, RD_PORT, VDACE, VDACOE, RBPU, TTL, VDD, VSS</p> <p>To Analog to Digital Converter and Comparators</p> |

TABLE 3 (cont'd)

| PIN NAME | EXEMPLARY BLOCK CIRCUITRY |
|----------|---|
| RB2/AN6 | <p>RB2/AN6</p> <p>WPUB Reg, PORTB Reg, TRIS Reg, ANSEL Latch, IOCB Reg</p> <p>Data bus, WR_WPUB, WR_PORT, WR_TRIS, RD_TRIS, WR_ANSEL, WR_IOCBL, RD_PORT, RBPU</p> <p>V_{DD}, V_{SS}, weak pull-up, weak pull-down</p> <p>To Analog to Digital Converter</p> |

TABLE 3 (cont'd)

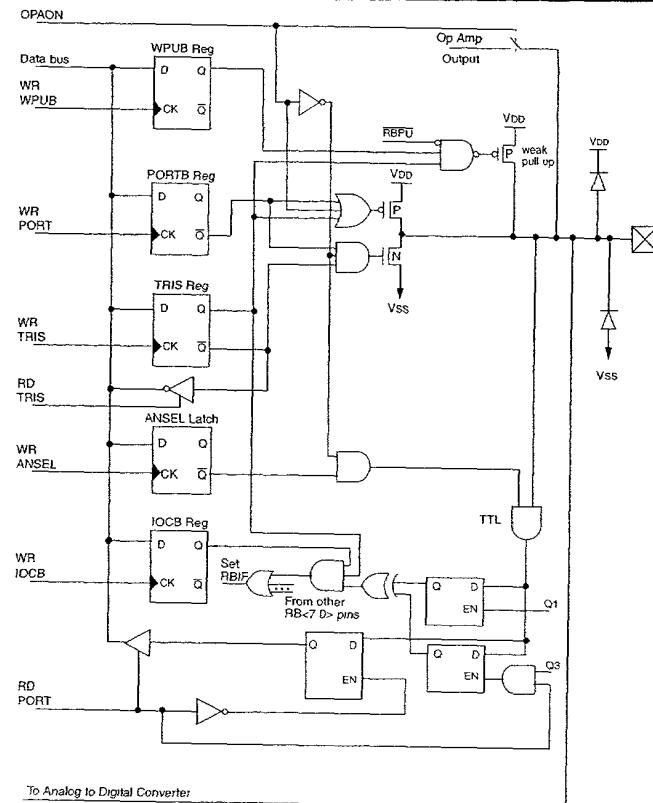
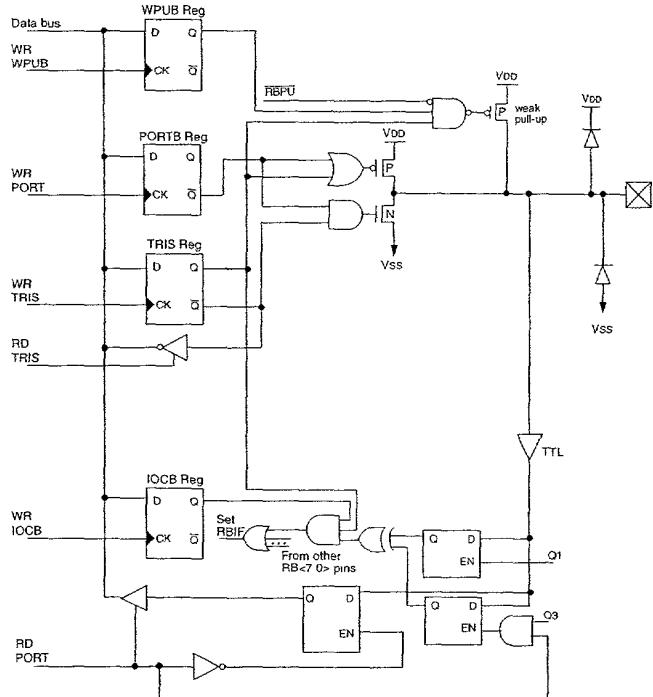
| PIN NAME | EXEMPLARY BLOCK CIRCUITY |
|-------------|---|
| RB3/AN7/OPA |  <p>OPAON</p> <p>Data bus, WR_WPUB, PORTB_Reg, TRIS_Reg, ANSEL_Latch, IOCB_Reg, RD_PORT, Op Amp Output, VDD, VSS, TTL, weak pull-up.</p> <p>To Analog to Digital Converter</p> |
| RB4 AND RB5 |  <p>WR_WPUB, PORTB_Reg, TRIS_Reg, IOCB_Reg, RD_PORT, VDD, VSS, TTL, weak pull-up.</p> |

TABLE 3 (cont'd)

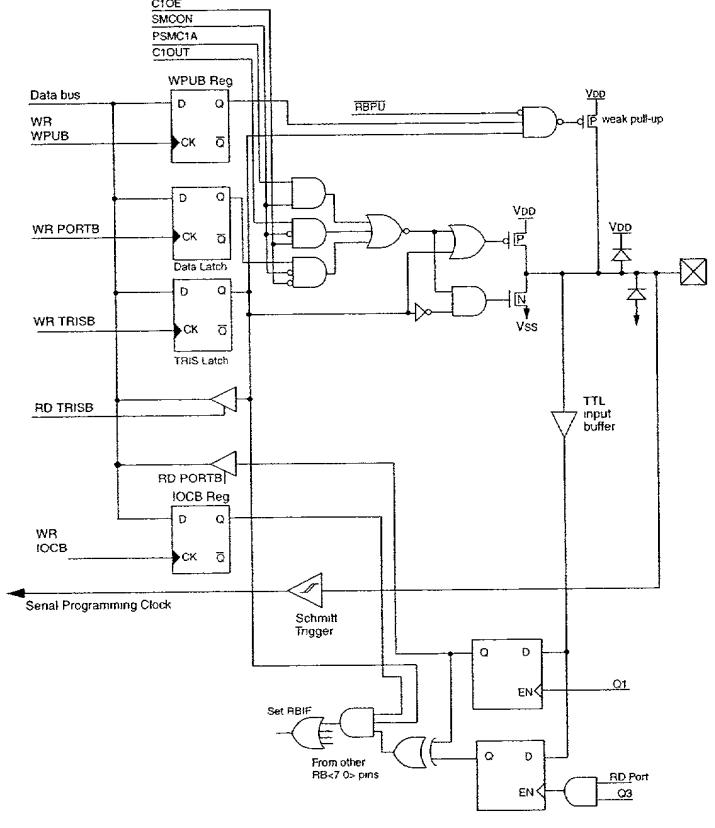
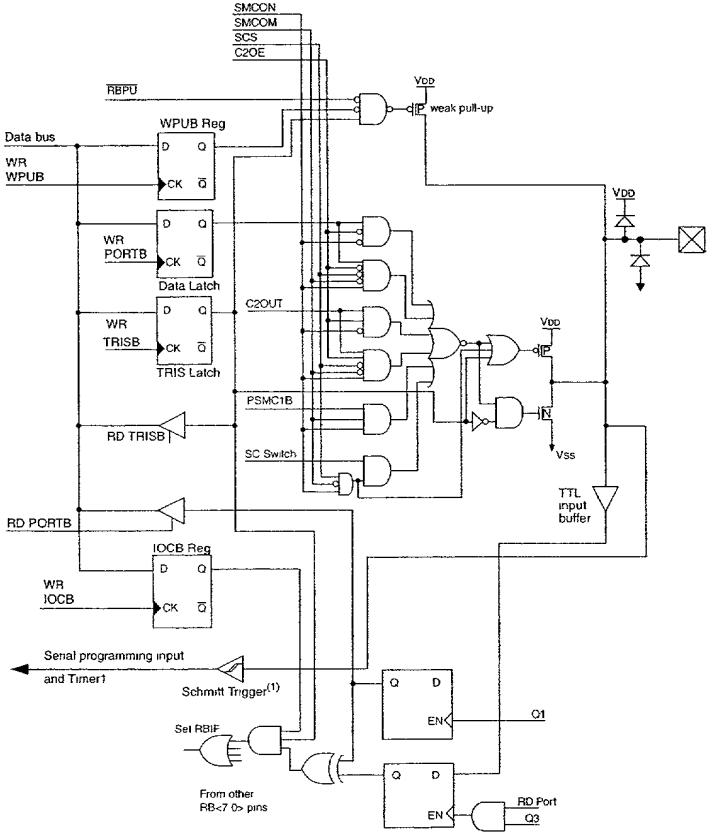
| PIN NAME | EXEMPLARY BLOCK CIRCUITRY |
|---------------|--|
| RB6/C1/PSMC1A |  <p>The diagram illustrates the internal logic for pin RB6/C1/PSMC1A. It features a complex arrangement of flip-flops, logic gates, and buffers. Key components include:</p> <ul style="list-style-type: none"> WR Path: A 3-to-1 multiplexer (MUX) selects between the Data bus and WR_WPUB. The MUX is controlled by C1OE, SMC0N, PSMC1A, and C1OUT. The output of the MUX is connected to a D flip-flop (WR_WPUB Reg) with CK from RD PORTB. The Q output of this flip-flop is connected to the RD PORTB input of a second D flip-flop (Data Latch). The Q output of the Data Latch is connected to the RD TRISB input of a third D flip-flop (TRIS Latch). The Q output of the TRIS Latch is connected to RD TRISB. RD Path: RD TRISB is connected to RD PORTB. RD PORTB is connected to a D flip-flop (RD PORTB Reg) with CK from WR IOCB. The Q output of this flip-flop is connected to the RD Port Q3 output. IOCB Path: WR IOCB is connected to the RD PORTB Reg's CK input. RD PORTB is also connected to a Schmitt Trigger, which is connected to a D flip-flop (Set RBIF). The Set RBIF output is connected to the RD Port Q3 output. Power and Control: The circuit includes a TTL input buffer, a weak pull-up, and a weak pull-down. Power supplies VDD and VSS are connected to various nodes. A Serial Programming Clock is shown as an input to the RD PORTB Reg and the Schmitt Trigger. Other: A note indicates that the Set RBIF output is also connected to other RB<7> O pins. |

TABLE 3 (cont'd)

| PIN NAME | EXEMPLARY BLOCK CIRCUITRY |
|-------------------|---|
| RB7/C2/PSMC1B/T1G |  |